IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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In re application of: Rajski et al.
Application No. 10/781,031
Filed: February 17, 2004
Confirmation No. 2828
For: METHOD FOR SYNTHESIZING LINEAR FINITE STATE MACHINES
Examiner: David H. Malzahn
Art Unit: 2193
Attorney Reference No. 1011-67627-01

CERTIFICATE OF MAILING

I hereby certify that this paper and the documents referred to as being attached or enclosed herewith are being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: MAIL STOP RCE, COMMISSIONER FOR PATENTS, P.O. BOX 1450, ALEXANDRIA, VA 22313-1450 on the date shown below.

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INFORMATION DISCLOSURE STATEMENT PURSUANT TO 37 C.F.R. § 1.97(b)(4)

Listed on the accompanying form PTO-1449 and enclosed herewith are several English-language and/or non-English-language documents. Applicants respectfully request that these documents be listed as references cited on the issued patent.

Further, several foreign language documents are cited in the accompanying form PTO-1449. Specifically, Japanese Patent Publication Nos. 63-286780, 03-012573, 05-249197, 07-174822, 08-015382, and 11-264860 are cited. Japanese Patent Publication No. 63-286780 describes a fault detecting system and fault detecting device. Japanese Patent Publication No. 03-012573 describes a logic circuit testing device having a test data changing circuit. Japanese Patent Publication No. 05-249197 describes an incorporated self-test circuit. Japanese Patent Publication No. 07-174822 describes a semiconductor integrated circuit device. Japanese Patent Publication No. 08-015382 describes a circuit incorporating a self test function. Japanese Patent Publication No. 11-264860 describes an output circuit of a semiconductor device with test mode.

Copies of United States patents and United States published patent applications do not have to be provided to the Patent Office (37 C.F.R. 1.98(a)(2)(ii)). Copies of unpublished U.S. applications do not have to be provided, as long as the application is available on PAIR, as this requirement of 37 C.F.R. § 1.98(a)(2)(iii) has been waived by the United States Patent and Trademark Office pursuant to the Official Gazette Notice on October 19, 2004 (1287 OG 163). Applicants will provide copies of such patents or applications upon request.

Applicants filed this Information Disclosure Statement ("IDS") before the mailing of a first Office action after the filing of a request for continued examination. As a result, no fee should be required to file this IDS. However, if the Patent Office determines that a fee is required for Applicants to file this IDS, please charge any such fees, or credit overpayment, to Deposit Account No. 02-4550.

The filing of this IDS shall not be construed to be an admission that the information cited in the statement is, or is considered to be, prior art or otherwise material to patentability as defined in 37 C.F.R. §1.56.

Respectfully submitted,

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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First Named Inventor	Rajski
Art Unit	2193
Examiner Name	David H. Malzahn

U.S. PATENT DOCUMENTS

Copies of U.S. Patent documents do not need to be provided, unless requested by the Patent and Trademark Office. For patents, provide the patent number and the issue date. For published U.S. applications, provide the publication number and the publication date. For unpublished pending patent applications, provide the application number and the filing date.

Examiner's Initials*	Cite No. (optional)	Number	Publication Date	Name of Applicant or Patentee
		5,072,178	12.10.1991	Matsumoto
		5,642,362	6.24.1997	Savir
		5,717,701	2.10.1998	Angelotti et al.
		6,590,929	7.8.2003	Williams

FOREIGN PATENT DOCUMENTS

Examiner's Initials*	Cite No. (optional)	Country	Number	Publication Date	Name of Applicant or Patentee
		Japan	63-286780 (w/English abstract)	11.24.1988	Iwasaki et al.
		Japan	03-012573 (w/English abstract)	1.21.1991	Matsumoto
		Japan	05-249197 (w/English abstract)	9.28.1993	Ikenaga et al.
		Japan	07-174822 (w/English abstract)	7.14.1995	Kondou
		Japan	08-015382 (w/English abstract)	1.19.1996	Hiraide et al.
		Europe	0 549 949	3.11.1998	Ikenaga et al.
		Japan	11-264860 (w/English abstract)	9.28.1999	Kitamura

Examiner's Initials*	Cite No. (optional)	OTHER DOCUMENTS
		Konemann et al., "Built-In Logic Block Observation Techniques," *IEEE Test Conference*, 6 pp. (1979).

EXAMINER SIGNATURE:	DATE CONSIDERED:

* Examiner: Initial if reference considered, whether or not in conformance with MPEP 609. Draw line through cite if not in conformance and not considered. Include copy of this form with next communication to applicant.